reads executed, as reasonable exhaustion of all opportunity for a successful read is better than a fatal error.

There have been disclosed and described herein preferred and alternate embodiments of a new and unique synchronous read channel which include a sequence detector with a flexible architecture capable of implementing a broad range of partial response polynomials. While an embodiment of the present invention which supports only one or two partial response channels would be highly useful, the detector used in the preferred embodiment of the present invention supports a broad class of partial response channels, including but not limited to PR4 (1,7), EPR4 (1,7) and EEPR (1,7). While the sequence detector is normally operative upon a read, the output of a digital peak detector may be enabled as the output of the read channel if desired. These and other inventive features of the invention will be apparent from the preceding description.

Thus while a preferred and alternate embodiments of the present invention has been disclosed and described in detail herein, it will be obvious to those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope thereof.

What is claimed is:

1. An integrated circuit synchronous read channel for receiving digitized read signals representing digitized

samples of a read signal of a magnetic storage device and recovering digital data represented thereby comprising:

a digital peak detector for detecting characteristics of the digitized read signals indicative of storage media transitions;

timing recovery circuitry responsive to the digitized read signals and the output of the digital peak detector to provide a timing control signal for controlling the timing of digitized samples of the read signal;

a sequence detector responsive to the digitized read signals for receiving a stream of the digitized read signals and determining a corresponding sequence of binary digital signals likely to be represented thereby;

an RLL(d,k) decoder for providing a run length limited decoded output by decoding the sequence of binary digital signals from the sequence detector, or to provide a run length limited decoded output by decoding a sequence of binary digital signals from the digital peak detector;

controllable means for directing either the sequence of binary digital signals from the sequence detector or an output from the digital peak detector to the RLL(d,k) decoder.

2. The integrated circuit synchronous read channel of claim 1 further comprised of digital pulse shaping filter circuitry for modification of the digitized read signals prior to receipt thereof by at least one of (i) the sequence

detector, (ii) digital peak detector and (iii) the timing recovery circuitry.

3. The integrated circuit synchronous read channel of claim 2 further comprised of delay means for delaying the coupling of the digitized read signals to the digital peak detector or the timing recovery circuitry to match the delay of the coupling of the digitized read signals to the timing recovery circuitry or the digital peak detector, respectively, imposed by the digital pulse shaping filter.

4. The integrated circuit synchronous read channel of claim 2 wherein the digital pulse shaping filter circuitry includes variable filter parameters.

5. The integrated circuit synchronous read channel of claim 2 wherein the digital pulse shaping filter circuitry includes programmable filter parameters.

6. The integrated circuit synchronous read channel of claim 1 further comprising spectrum smoothing filter circuitry for filtering the digitized read signals prior to processing by the sequence detector.

7. The integrated circuit synchronous read channel of claim 1 wherein the sequence detector processes two digitized read signals at a time, the two digitized read signals

representing digitized samples of a read signal of a magnetic storage device during two successive channel bit times.